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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/596,129	06/16/2000	Manfred Reithinger	00P7685US	2660

7590 04/01/2002

Siemens Corporation
Intellectual Property Department
186 Wood Avenue South
Iselin, NJ 08830

EXAMINER
CAO, PHAT X

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/596,129	Reithinger et al.
Examiner	**Art Unit**
Phat X. Cao	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Feb 1, 2002*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above, claim(s) *8 and 9* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-7* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
18) ☐ Interview Summary (PTO-413) Paper No(s). _____
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group I, claims 1-7 in Paper No. 6 is acknowledged.

Drawings

2. Figures 1-2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

4. Claim 5 recites the limitation "such package" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 5-6 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Murari et al (US. 5,696,404).

With respect to claims 1, 6 and 7, Murari, in Fig. 2, discloses a semiconductor wafer having a plurality of integrated circuit chips 2 thereon, such chips being separated by separating regions in the fractional portion of the wafer; a plurality of sets of electrical components D and R, each set being associated with and adjacent to a corresponding one of the chips 2; and an electrical conductor 12 electrically connecting the plurality of electrical selected one or ones of the electrical components to the chips with portions of the electrical conductor 12 spanning the separating regions between the chips 2 in the fractional portion of the wafer.

With respect to claim 5, Murari (Fig. 5) further discloses a dielectric member 14 having the electrical conductor 12 thereon (the connecting conducting line bus 12 can be individual metalization strips 13, see column 4, lines 11-20).

7. Claims 1-4 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Tagaya (JP. 6-13447).

Tagaya, in Fig. 4 and abstract, discloses a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating region in the fractional

portion of the wafer; a plurality of sets of electrical components 10, each set being associated with, and adjacent to a corresponding one of the chips; and an electrical conductor 13 electrically connecting the plurality of electrical selected one of the electrical components 10 to the chips with portion of the electrical conductor 13 spanning the separating regions 16 between the chips in the fractional portion of the wafer; wherein each one of the electrical components 10 is voltage signal generators (see abstract) and is disposed in the separating region 16.

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

9. Claims 1-4 and 6-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Egawa (US. 6,066,886).

Egawa, in Figs. 1 and 3, discloses a semiconductor comprising: a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the fractional portion of the wafer; a plurality of sets of electrical components 4, each set being associated with, and adjacent to, a corresponding one of the chips; and an electrical conductor PX (see Fig. 3) electrically connecting the plurality of electrical selected one or ones of the electrical components 4 to the chips with portions of the electrical conductor spanning the separating regions between the chips in the fractional portion of

the wafer (see Figs. 3 and 4); wherein the electrical components 4 are voltage signal generators, and each of the electrical components 4 has a plurality of different electrical components.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (703) 308-4917. The Examiner can normally be reached on Monday through Thursday. If attempts to reach the Examiner by telephone are unsuccessfully, the Examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. Group 2800 fax number is (703) 308-7722 or (703) 308-7724.

PHAT X. CAO
PRIMARY EXAMINER

PC
March 21, 2002